

Multiresolution Image Sensor Using Switched Capacitor Circuits

Sabrina Kemeny, Bedabrata Pain, Eric Fossum,
Larry Matthies, and Roger Panicacci

Jet Propulsion Laboratory
California Institute of Technology

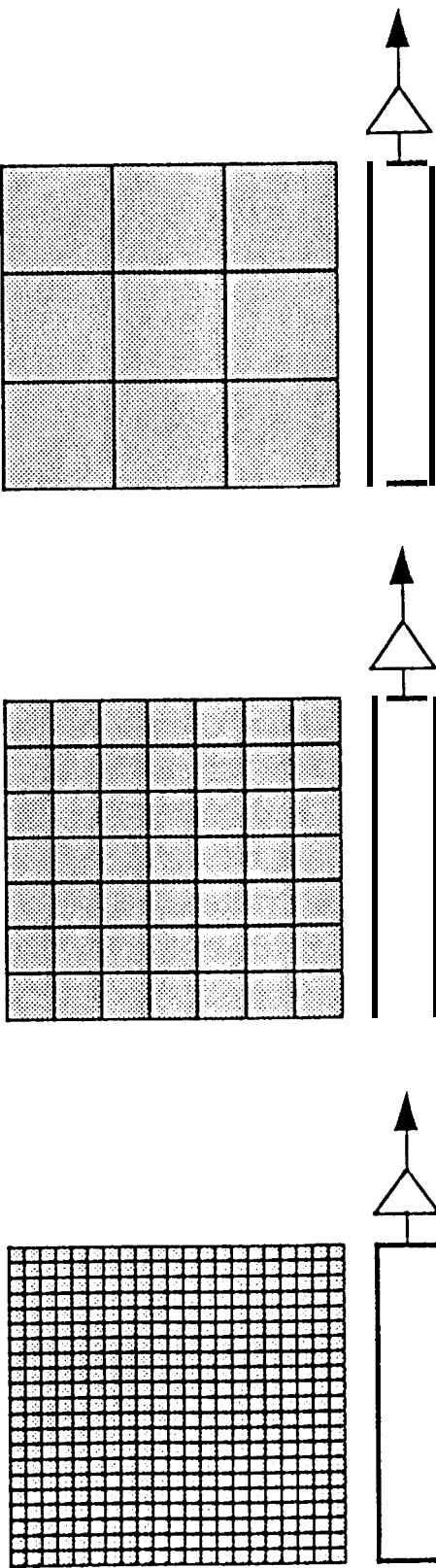
10-17-94

1994 International CMOS Camera Workshop

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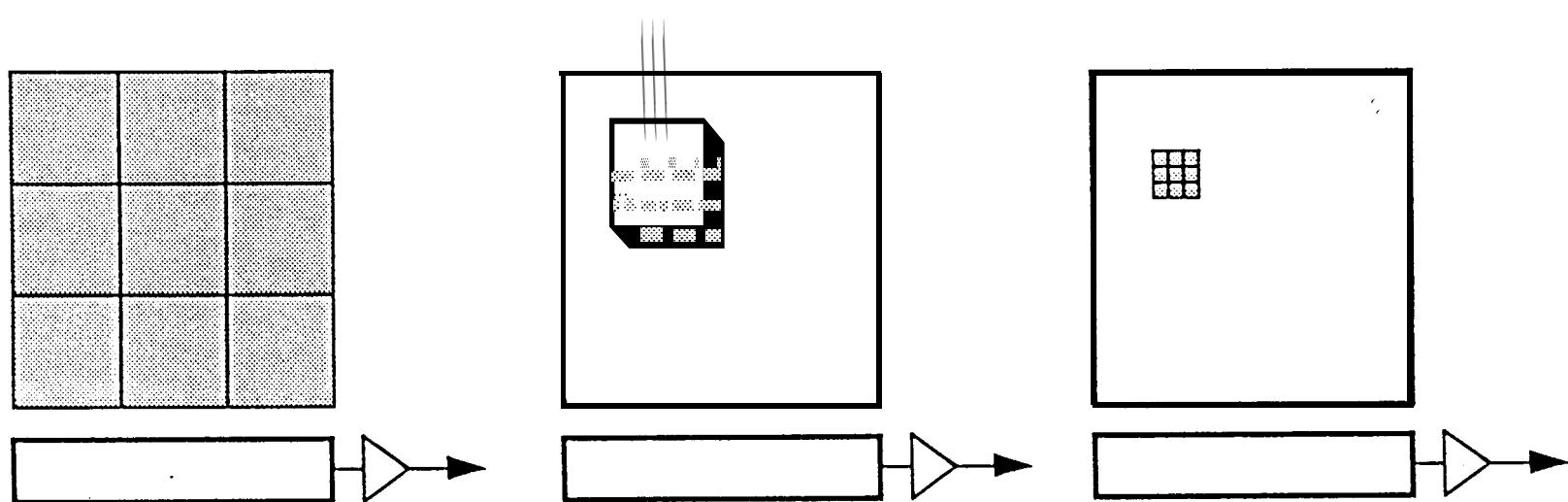
Multiresolution APS

Multi resolution Readout Sensor: Pyramidal Readout



Read Out Array at Desired Resolution

Multiresolution Readout Sensor: Window Readout



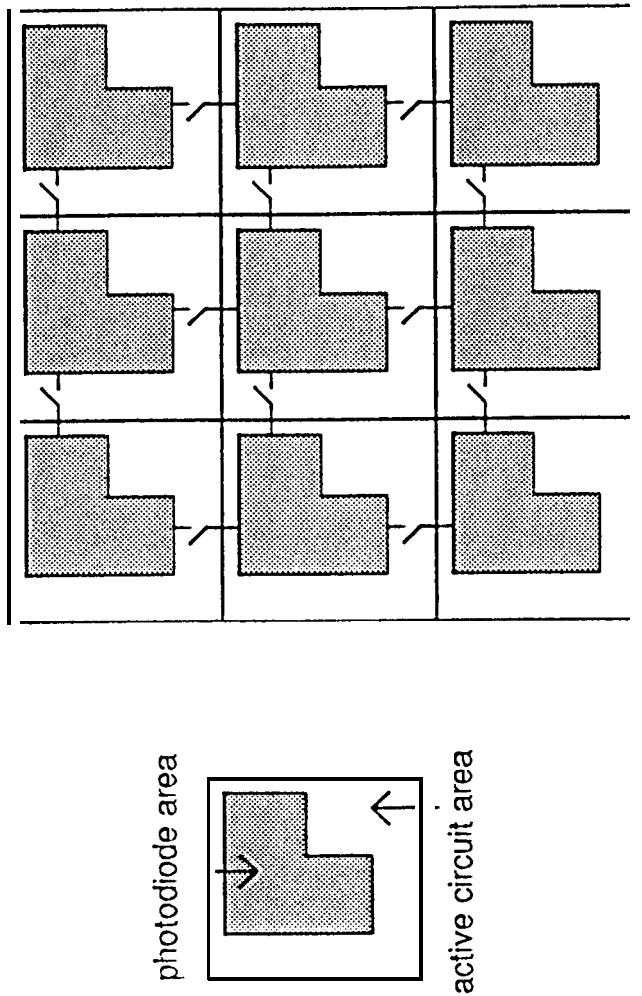
Applications

- Autonomous Navigation
- Pattern Recognition
- Target Tracking
- Progressive Transmission of Compressed Images
- Biological Vision Modeling

→ **POL**

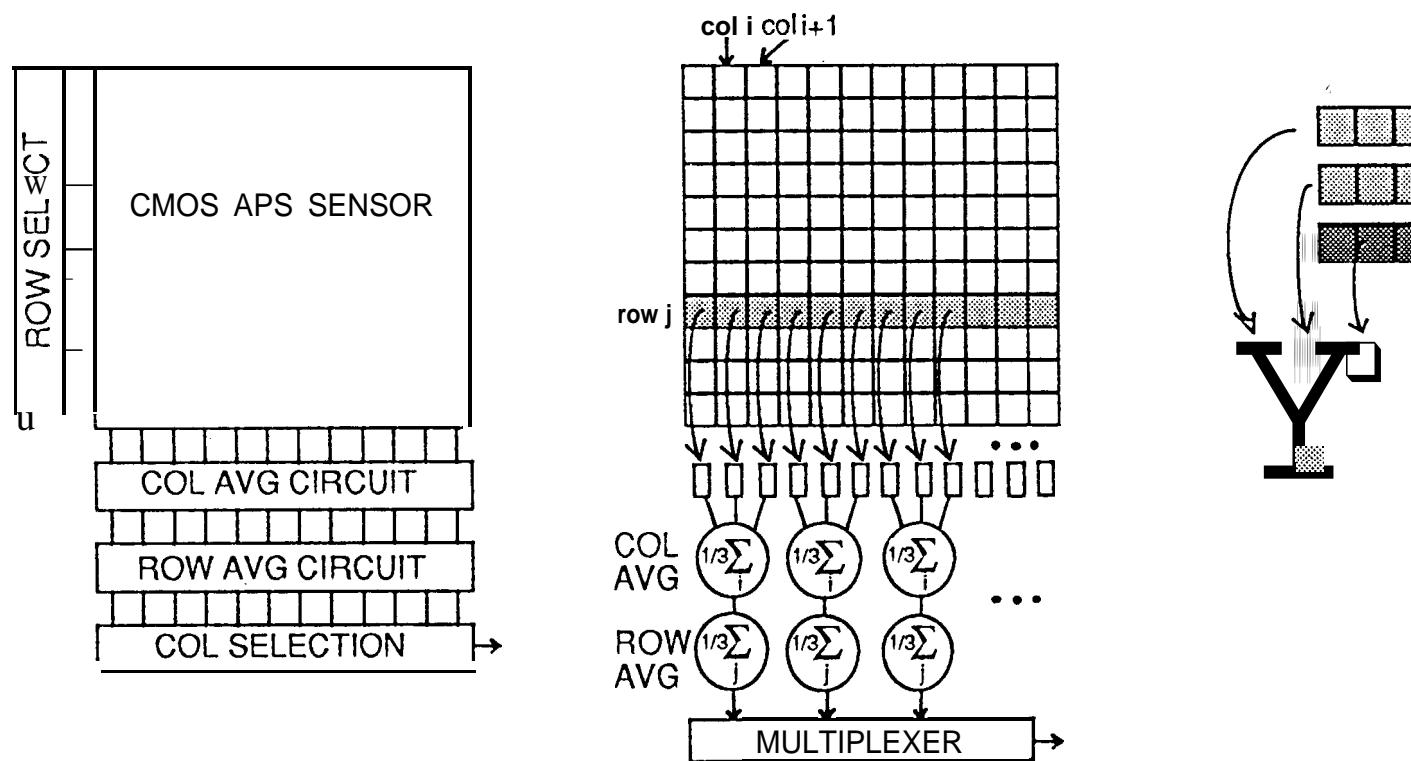
Multiresolution APS

Spatial y Paralelo Approach



- Photodiodes interconnected through a set of programmable switches
 - Capacitance scales nearly with increasing area realizing block averaging

Column Parallel Approach

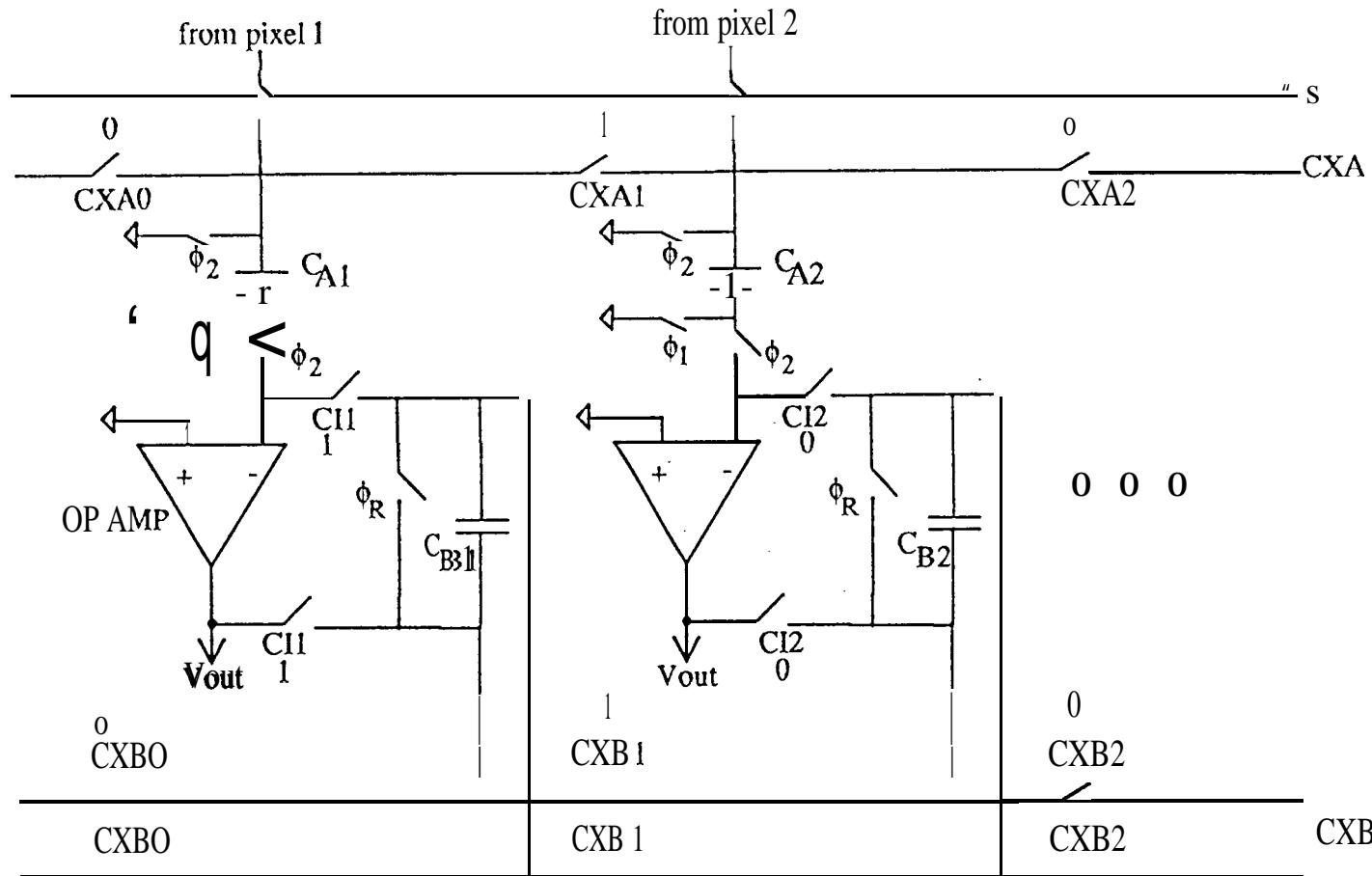


Parallel block averaging of kernels followed by serial readout

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Multiresolution APS

Switched Capacitor Implementation



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Multiresolution APS

Project Specification and Performance

Array Size:

Pixel size:

Access:

Fill factor:

Programmable Window Size:

256 × 256

19.2 μm

.2 μm CMOS

30 %

n rows × m columns

n,m = 1 ... ,256 m>=n

Frame Rate:

Full resolution

Lower solution

e.g. 64 × 64

30 Hz ($T_f = 33.3\text{ms}$)

{ $T_f/n + n(\text{sma overhead})$ }⁻¹

{ $33.3\text{ms}/4 + 4(8\mu\text{s})$ }⁻¹ = 1 9.7 Hz

Dynamic Range:

75 dB

→ PTL

Multiresolution APS

Recursion Relation

$$V_{out}(k) = \frac{\sum_{i=1}^{k-1} C_{Bi}}{\sum_{i=1}^k C_{Bi}} V_{out}(k-1) + \frac{C_{Ai}}{\sum_{i=1}^k C_{Bi}} V_{in}(k)$$
$$V_{in}(k) = \bar{V}_{k, \circ}$$

2x2 Example

$$V_{out}(2) = \frac{1}{2} V_{out}(1) + \frac{1}{2} \bar{V}_{2,2}$$
$$V_{out}(1) = \frac{0}{1} V_{out}(0) + \frac{1}{1} \bar{V}_{1,2}$$
$$V_{out}(0) = \circ$$

therefore

$$V_{out}(2) = \frac{1}{2} \bar{V}_{1,2} + \frac{1}{2} \bar{V}_{2,2}$$
$$= \frac{1}{2} \left(\frac{V_{1,1} + V_{1,2}}{2} \right) + \frac{1}{2} \left(\frac{V_{2,1} + V_{2,2}}{2} \right)$$
$$= \frac{V_{1,1} + V_{1,2} + V_{2,1} + V_{2,2}}{4}$$

where k is the cycle index
and n is the kernel size

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Multiresolution APS

Switched Capacitor Timing

